INTEGRATED CIRCUITS

DATA SHEET

TDA8440
Switch for CTV receivers

Product specification
File under Integrated Circuits, IC02

November 1985

Philips
Semiconductors

PHILIPS

GENERAL DESCRIPTION

The TDA8440 is a versatile video/audio switch, intended to be used in CTV receivers equipped with an AUXILIARY VIDEO/AUDIO plug.

It provides two 3-state switches for audio channels and one 3-state switch for the video channel and a video amplifier with selectable gain (times 1 or times 2).

The integrated circuit can be used in conjunction with a microcontroller from the MAB8400 family, and is controlled via a bidirectional I^2C bus. Sufficient sub-addressing is provided for the I^2C bus mode. It can also be controlled directly by d.c. switching signals.

Features

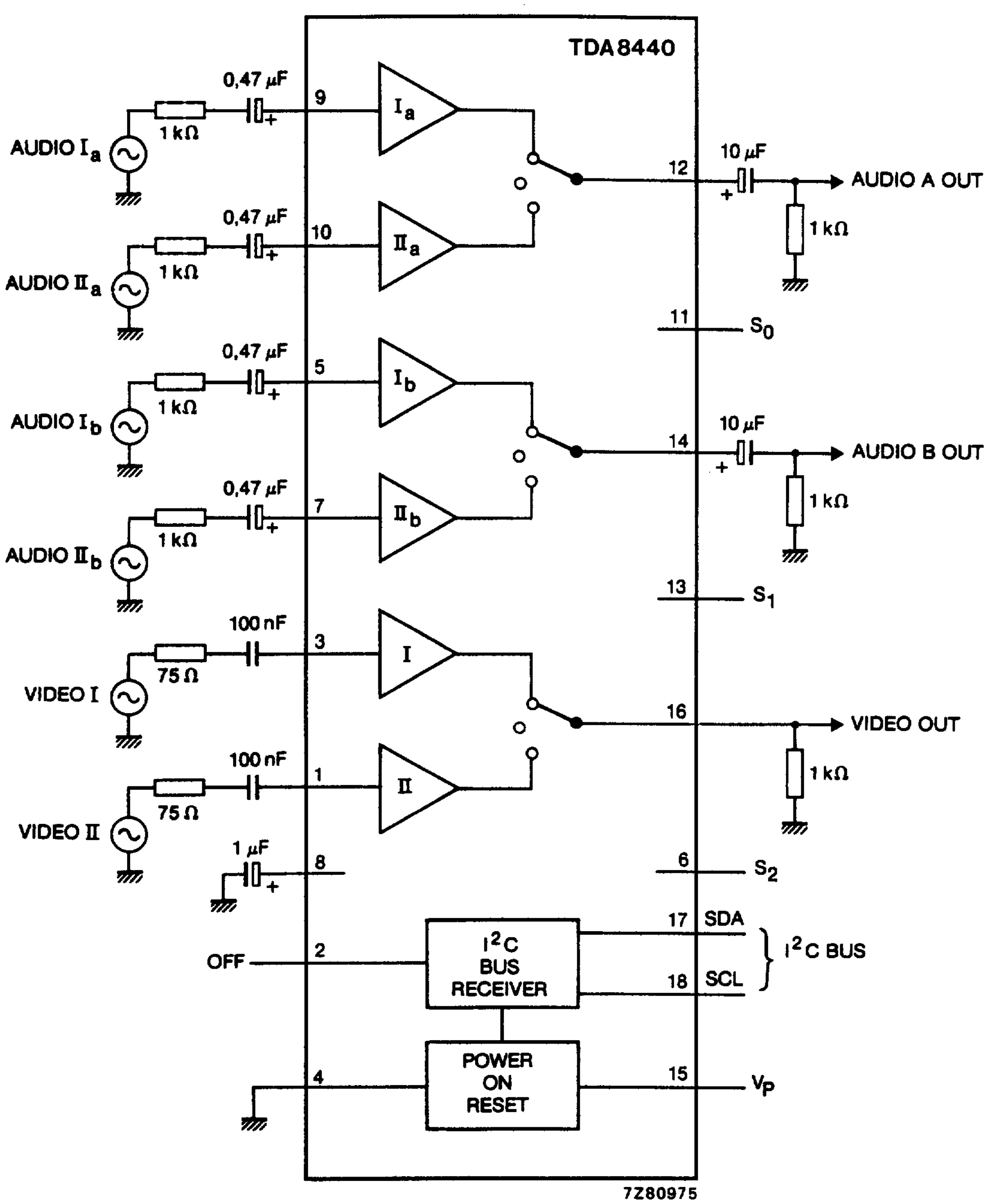
- Combined analogue and digital circuitry gives maximum flexibility in channel switching
- 3-state switches for all channels
- Selectable gain for the video channels
- Sub-addressing facility
- I^2C bus or non-I^2C bus mode (controlled by d.c. voltages)
- Slave receiver in the I^2C bus mode
- External OFF command
- System expansion possible up to 7 devices (14 sources)
- Static short-circuit proof outputs

QUICK REFERENCE DATA

Supply voltage range	V_{15-4}		10 to 13,2	V
Supply current (without load)	I_{15}	typ.	33	mA
		max.	50	mA
Storage temperature	T_{stg}	max.	+ 125	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102); SOT102-1; 1996 November 19.



S0, S1, S2 and OFF (pins 11, 13, 6 and 2) connected to V_P or GND.
If more than 1 device is used, then the outputs and the pins 8 (bias decoupling of the audio inputs) may be connected in parallel.

Fig.1 Block diagram and test circuit.

FUNCTIONAL DESCRIPTION

The TDA8440 is a monolithic system of switches and can be used in CTV receivers equipped with an AUXILIARY VIDEO/AUDIO plug.

The IC incorporates 3-state switches; they comprise:

a) An electronic video switch with selectable gain (times 1 or times 2) for switching between an internal video signal (from the IF amplifier) and an AUXILIARY input signal.

b) Two electronic audio switches, for two sound channels (stereo or dual language), for switching between internal audio sources and signals from the AUXILIARY VIDEO/AUDIO plug.

A selection can be made between two input signals and an OFF-state. The OFF-state is necessary if more than one TDA8440 device is used.

The SDA and SCL pins can be connected to the I^2C bus or to d.c. switching voltages. Inputs S_0 (pin 11), S_1 (pin 13), and S_2 (pin 6) are used for selection of sub-addresses or switching to the non-I^2C mode. Inputs S_0, S_1 and S_2 can be connected to the supply voltage (H) or to ground (L). In this way no peripheral components are required for selection.

Table 1 Sub-addressing

S_2	S_1	S_0	SUB-ADDRESS		
			A_2	A_1	A_0
L	L	L	0	0	0
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	non I^2C addressable		

NON-I^2C BUS CONTROL

If the TDA8440 switching device has to be operated via the AUXILIARY VIDEO/AUDIO plug, inputs S_2, S_1 and S_0 must be connected to the supply line (12 V).

The sources (internal and external) and the gain of the video amplifier can be selected via the SDA and SCL pins with the switching voltage from the AUXILIARY VIDEO/AUDIO plug:

- Sources I are selected if SDA = 12 V (external source)
- Sources II are selected if SDA = 0 V (TV mode)
- Video amplifier gain is 2 × if SCL = 12 V (external source)
- Video amplifier gain is 1 × if SCL = 0 V (TV mode)

If more than one TDA8440 device is used in the non-I^2C bus system, the OFF pin can be used to switch off the desired devices. This can be done via the 12 V switching voltage on the AUXILIARY VIDEO/AUDIO plug.

- All switches are in the OFF position if OFF = H (12 V)
- All switches are in the selected position via SDA and SCL pins if OFF = L (0 V)

I²C BUS CONTROL

Detailed information on the I²C bus is available on request.

Table 2 TDA8440 I²C bus protocol.

STA	A_6	A_5	A_4	A_3	A_2	A_1	A_0	R/W	AC	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	AC	STO

STA = start condition
A_6 = 1 Fixed address bits
A_5 = 0 Fixed address bits
A_4 = 0 Fixed address bits
A_3 = 1 Fixed address bits
A_2 = sub-address bit, fixed via S_2 input
A_1 = sub-address bit, fixed via S_1 input
A_0 = sub-address bit, fixed via S_0 input
R/W = read/write bit (has to be 0, only write mode allowed)
AC = acknowledge bit (= 0) generated by the TDA8440
D_7 = 1 audio Ia is selected to audio output a
D_7 = 0 audio Ia is not selected
D_6 = 1 audio IIa is selected to audio output a
D_6 = 0 audio IIa is not selected
D_5 = 1 audio Ib is selected to audio output b
D_5 = 0 audio Ib output is not selected
D_4 = 1 audio IIb is selected to audio output b
D_4 = 0 audio IIb is not selected
D_3 = 1 video I is selected to video output
D_3 = 0 video I is not selected
D_2 = 1 video II is selected to video output
D_2 = 0 video II is not selected
D_1 = 1 video amplifier gain is times 2
D_1 = 0 video amplifier gain is times 1
D_0 = 1 OFF-input inactive
D_0 = 0 OFF-input active
STO = stop condition

OFF FUNCTION

With the OFF input all outputs can be switched off (mode high ohmic), depending on the value of D_0.

D_0/OFF gating

D_0	OFF INPUT	OUTPUTS
0 (off input active)	H	OFF
0	L	in accordance with last defined D_7 - D_1 (may be entered while OFF = HIGH)
1 (off input inactive)	H	in accordance with D_7 - D_1
1	L	in accordance with D_7 - D_1

Power-on reset

The circuit is provided with a power-on reset function.

When the power supply is switched on an internal pulse will be generated that will reset the internal memory S_0, in the initial state all the switches will be in the off position and the OFF input is active (D_7 - D_0 = 0) (I^2C mode), position defined via SDA and SCL inputs (non-I^2C mode).

When the power supply decreases below 5 V a pulse will be generated and the internal memory will be reset. The behaviour of the switches will be the same as described above.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			MIN.	TYP.	MAX.	UNIT
Supply voltage	pin 15	V_P	–	–	14	V
Input voltage range	pin 17	V_{SDA}	–0,3	–	V_P + 0,3	V
	pin 18	V_{SCL}	–0,3	–	V_P + 0,3	V
	pin 2	V_{OFF}	–0,3	–	V_P + 0,3	V
	pin 11	V_{S0}	–0,3	–	V_P + 0,3	V
	pin 13	V_{S1}	–0,3	–	V_P + 0,3	V
	pin 6	V_{S2}	–0,3	–	V_P + 0,3	V
Video output current	pin 16	$-I_{16}$	–	–	50	mA
Storage temperature range	T_{stg}		–	–	+ 125	°C
Operating ambient temperature range	T_{amb}		0	–	+ 70	°C
Junction temperature	T_j		–	–	+ 150	°C

THERMAL RESISTANCE

PARAMETER	SYMBOL	VALUE	UNIT
From junction to ambient in free air	$R_{th\ j-a}$	50	K/W

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply					
Supply voltage	$V_{15\text{-}4}$	10	–	13,2	V
Supply current (without load)	I_{15}	–	37	50	mA
Video switch					
Input coupling capacitor	C_1C_3	100	–	–	nF
Voltage gain (times 1; SCL = L)	$A_{3\text{-}16}$	–1	0	+ 1	dB
(times 2; SCL = H)	$A_{3\text{-}16}$	+ 5	+ 6	+ 7	dB
Voltage gain (times 1; SCL = L)	$A_{1\text{-}16}$	–1	0	+ 1	dB
(times 2; SCL = H)	$A_{1\text{-}16}$	+ 5	+ 6	+ 7	dB
Input video signal amplitude (gain times 1)	$V_{3\text{-}4}$	–	–	4,5	V
Input video signal amplitude (gain times 1)	$V_{1\text{-}4}$	–	–	4,5	V
Output impedance	$Z_{16\text{-}4}$	–	7	–	Ω
Output impedance in ‘OFF’ state	$Z_{16\text{-}4}$	100	–	–	kΩ
Isolation (off state) (f_o = 5 MHz)		60	–	–	dB
Signal-to-noise ratio (note 3)	S/S + N	60	–	–	dB
Output top-sync level	$V_{16\text{-}4}$	2,4	2,8	3,2	V
Differential gain	G	–	–	3	%
Minimum crosstalk attenuation (note 2)	$V_{16\text{-}4}$	60	–	–	dB
Supply voltage rejection (note 4)	RR	36	–	–	dB
Bandwidth (1 dB)	B	10	–	–	MHz
Crosstalk attenuation for interference caused by bus signals (source impedance 75 Ω)	α	60	–	–	dB
Audio switch a and b					
Input signal level	$V_{9\text{-}4(rms)}$	–	–	2	V
	$V_{10\text{-}4(rms)}$	–	–	2	V
	$V_{5\text{-}4(rms)}$	–	–	2	V
	$V_{7\text{-}4(rms)}$	–	–	2	V
Input impedance	$Z_{9\text{-}4}$	50	100	–	kΩ
	$Z_{10\text{-}4}$	50	100	–	kΩ
	$Z_{5\text{-}4}$	50	100	–	kΩ
	$Z_{7\text{-}4}$	50	100	–	kΩ
Output impedance	$Z_{12\text{-}4}$	–	–	10	Ω
	$Z_{14\text{-}4}$	–	–	10	Ω
Output impedance (off state)	$Z_{14\text{-}4}$	100	–	–	kΩ

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Voltage gain	V_{9-12}	–1	0	+ 1	dB
	V_{10-12}	–1	0	+ 1	dB
	V_{5-14}	–1	0	+ 1	dB
	V_{7-14}	–1	0	+ 1	dB
Isolation (off state) (f = 20 kHz)		90	–	–	dB
Signal-to-noise ratio (note 5)	S/S + N	90	–	–	dB
Total harmonic distortion (note 7)	THD	–	–	0,1	%
Crosstalk attenuation for interferences caused by video signals (note 6)					
Weighted	α	80	–	–	dB
Unweighted	α	80	–	–	dB
Crosstalk attenuation for interferences caused by sinusoidal sound signals (note 6)	α	80	–	–	dB
Crosstalk attenuation for interferences caused by the bus signal (weighted) (source impedance = 1 kΩ)		80	–	–	dB
Supply voltage rejection	RR	50	–	–	dB
Bandwidth (–1 dB)	B	50	–	–	kHz
I^2C bus inputs/outputs SDA (pin 17) and SCL (pin 18)					
Input voltage HIGH	V_{IH}	3	–	V_P	V
Input voltage LOW	V_{IL}	–0,3	–	+ 1,5	V
Input current HIGH(1)	I_{IH}	–	–	10	µA
Input current LOW(1)	I_{IL}	–	–	10	µA
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Capacitance of SDA and SDL inputs, pins 17 and 18	C_I	–	–	10	pF
Sub-address inputs S_0 (pin 11), S_1 (pin 13), S_2 (pin 6)					
Input voltage HIGH	V_{IH}	3	–	V_P	V
Input voltage LOW	V_{IL}	–0,3	–	+ 0,4	V
Input current HIGH	I_{IH}	–	–	10	µA
Input current LOW	I_{IL}	–50	–	0	µA
OFF input (pin 2)					
Input voltage HIGH	V_{IH}	+3	–	V_P	V
Input voltage LOW	V_{IL}	–0,3	–	+ 0,4	V
Input current HIGH	I_{IH}	–	–	20	µA
Input current LOW	I_{IL}	–10	–	2	µA

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Bus free before start(11)	t_{BUF}	4	–	–	µs
Start condition set-up time	$t_{s(STA)}$	4	–	–	µs
Start condition hold time	$t_{h(STA)}$	4	–	–	µs
SCL, SDA LOW period	t_{LOW}	4	–	–	µs
SCL, HIGH period	t_{HIGH}	4	–	–	µs
SCL, SDA rise time	t_r	–	–	1	µs
SCL, SDA fall time	t_f	–	–	0,3	µs
Data set-up time (write)	$t_{s(DAT)}$	1	–	–	µs
Data hold time (write)	$t_{h(DAT)}$	1	–	–	µs
Acknowledge (from TDA8440) set-up time	$t_{s(CAC)}$	–	–	2	µs
Acknowledge (from TDA8440) hold time	$t_{h(CAC)}$	0	–	–	µs
Stop condition set-up time	$t_{s(STO)}$	4	–	–	µs

Notes to the characteristics

1. Also if the supply is switched off.
2. Caused by drive on any other input at maximum level, measured in B = 5 MHz, source impedance for the used input 75 Ω,

   $$\text{crosstalk} = 20\ \log\frac{V_{out}}{V_{IN}\ \max}$$

3. $S/N = 20\ \log\frac{V_O\ \text{video noise (p-p) (2 V)}}{V_O\ \text{noise rms B = 5 MHz}}$.
4. Supply voltage ripple rejection = $20\ \log\frac{V_r\ \text{supply}}{V_r\ \text{on output}}$ at f = max. 100 kHz.
5. $S/N = 20\ \log\frac{V_O\ \text{nominal (0,5 V)}}{V_O\ \text{noise B = 20 kHz}}$.
6. Caused by drive of any other input at maximum level, measured in B = 20 kHz, source impedance of the used input = 1 kΩ,

   crosstalk = $20\ \log\frac{V_{out}}{V_{in}\ \max}$ according to DIN 45405 (CCIR 468).

7. f = 20 Hz to 20 kHz.
8. All outputs are short-circuit proof (static).
9. The inputs and output (apart from SDA, SCL and OFF) withstand tests of MIL-STD-883 C. It is advisable to connected series resistors to these pins.
10. Timings $t_{S,\ DAT}$ and $t_{H,\ DAT}$ deviate from the I^2C bus specification. After reset has been activated, transmission may only be started after a 50 µs delay.
11. I^2C bus load conditions are as follows:
    4kΩ pull-up resistor to + 5 V; 200 pF to GND.
    All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

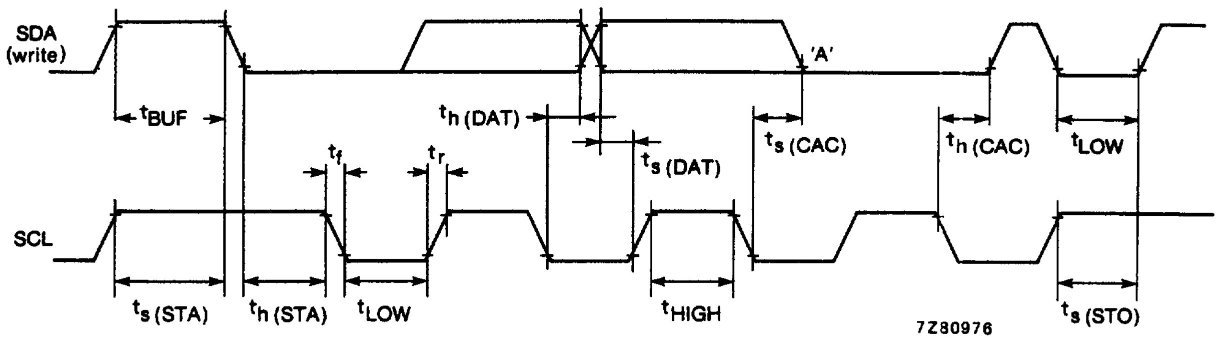
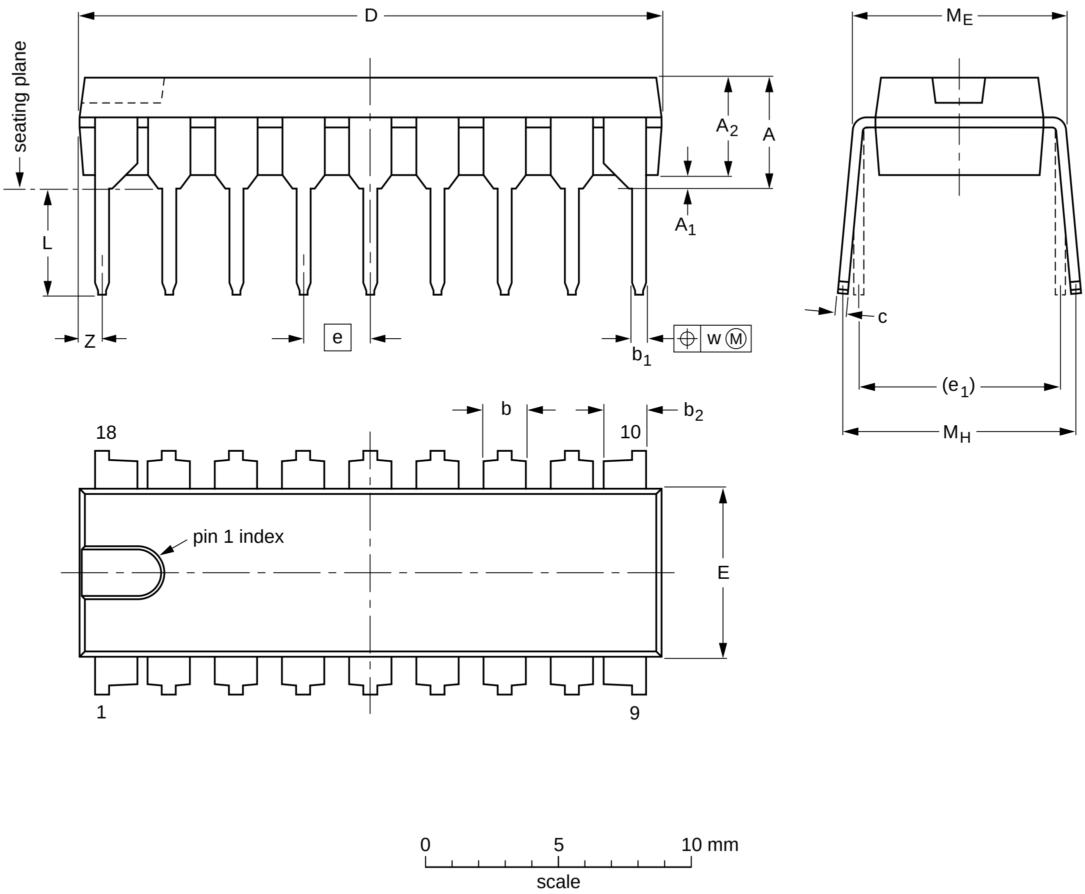


Fig.2 Timing diagram I^2C bus.

PACKAGE OUTLINE

DIP18: plastic dual in-line package; 18 leads (300 mil) **SOT102-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D [(1)]	E [(1)]	e	e_1	L	M_E	M_H	w	Z [(1)] max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	1.40 1.14	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	0.85
inches	0.19	0.020	0.15	0.055 0.044	0.021 0.015	0.055 0.044	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.033

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT102-1						~~93-10-14~~ 95-01-23

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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